ABSTRACT OF THE DISCLOSURE

An information processing system which reduces an access latency from a memory read request of a processor to a response thereto and also prevents reduction of the effective performance of a system bus caused by an increase in the access latency. In the information processing system, a memory controller is connected with the processor via a first bus and connected with a memory via a second bus, and a buffer memory is provided in the memory controller. The control circuit is controlled, before a memory access from the processor is carried out, to estimate an address to be possibly next accessed on the basis of addresses accessed in the past and to prefetch into the buffer memory, data stored in an address area continuous to the address and having a data size of twice or more an access unit of the processor.